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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,547	09/09/2003	Sheng Teng Hsu	SLA0746	3059
55286 7590 06/01/2007 SHARP LABORATORIES OF AMERICA, INC. C/O LAW OFFICE OF GERALD MALISZEWSKI P.O. BOX 270829 SAN DIEGO, CA 92198-2829			EXAMINER PERKINS, PAMELA E	
			ART UNIT 2822	PAPER NUMBER
			MAIL DATE 06/01/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/659,547	Applicant(s) HSU ET AL.	
	Examiner Pamela E. Perkins	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-11,13-19 and 21-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-3,5-11 and 13-19 is/are allowed.
- 6) ☒ Claim(s) 21-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the filing of the amendment on 8 March 2007. Claims 1-3, 5-11, 13-19 and 21-27 are pending; claims 4, 12, and 20 have been cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe (5,418,389).

Watanabe discloses a ferroelectric transistor where source, drain, and channel regions are formed in a substrate; a gate structure including: a conductive oxide layer

(3) overlying the channel region having a lattice structure; a ferroelectric material layer (4) overlying the conductive oxide layer (3) having a lattice structure matching the conductive oxide lattice structure; and, a top electrode conductive layer (5) overlying the ferroelectric material layer (4) (Fig. 3; col. 3, lines 34-50; col. 11, line 25 thru col. 12, line 14).

Referring to claim 23, wherein the ferroelectric material layer has a perovskite crystal lattice structure (abstract).

Claims 24 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Moon (6,744,374).

Referring to claims 24 and 26, Moon discloses a ferroelectric transistor consisting of source (3), drain (3), and channel regions formed in a substrate (1); a gate structure (20) including: a non-silicon-containing conductive oxide layer (11a) overlying the channel region; a ferroelectric material layer (12a) overlying the conductive oxide layer (11a); and, a top electrode conductive layer (13a) overlying the ferroelectric material layer (12a) (Fig. 2; col. 4, lines 43-54).

Claim 27 is rejected under 35 U.S.C. 102(e) as being anticipated by Willer et al. (6,538,273).

Willer et al. disclose a ferroelectric transistor consisting of source (2), drain (2), and channel (3) regions formed in a substrate (1); a gate structure including: a conductive oxide layer (4₁) overlying the channel (3) region; a bottom electrode

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conductive layer (4₂) overlying the conductive oxide layer (4₁); a ferroelectric material layer (5) overlying the bottom electrode conductive layer (4₂); and, a top electrode conductive layer (6) overlying the ferroelectric material layer (5) (Fig. 1; col. 5, lines 6-63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Willer et al.

Watanabe discloses the subject matter claimed above except wherein the gate structure further includes a bottom electrode conductive layer interposed between the conductive oxide layer and the ferroelectric material layer.

Willer et al. disclose a ferroelectric transistor consisting of source (2), drain (2), and channel (3) regions formed in a substrate (1); a gate structure including: a conductive oxide layer (4₁) overlying the channel (3) region; a bottom electrode conductive layer (4₂) overlying the conductive oxide layer (4₁); a ferroelectric material layer (5) overlying the bottom electrode conductive layer (4₂); and, a top electrode conductive layer (6) overlying the ferroelectric material layer (5) (Fig. 1; col. 5, lines 6-63).

Since Watanabe and Willer et al. are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Willer et al. would have been recognized in the pertinent art of Watanabe. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Watanabe by the gate structure further includes a bottom electrode conductive layer interposed between the conductive oxide layer and the ferroelectric material layer by Willer et al. to improve punch-through voltage (col. 1, lines 43-64).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moon in view of Willer et al.

Moon discloses the subject matter claimed above except wherein the gate structure further includes a bottom electrode conductive layer interposed between the conductive oxide layer and the ferroelectric material layer.

Willer et al. disclose a ferroelectric transistor consisting of source (2), drain (2), and channel (3) regions formed in a substrate (1); a gate structure including: a conductive oxide layer (4₁) overlying the channel (3) region; a bottom electrode conductive layer (4₂) overlying the conductive oxide layer (4₁); a ferroelectric material layer (5) overlying the bottom electrode conductive layer (4₂); and, a top electrode conductive layer (6) overlying the ferroelectric material layer (5) (Fig. 1; col. 5, lines 6-63).

Since Moon and Willer et al. are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Willer et al. would have

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been recognized in the pertinent art of Moon. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Moon by the gate structure further includes a bottom electrode conductive layer interposed between the conductive oxide layer and the ferroelectric material layer by Willer et al. to improve punch-through voltage (col. 1, lines 43-64).

Allowable Subject Matter

Claims 1-3, 5-11 and 13-19 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not anticipate, teach, or suggest a conductive oxide layer overlying a substrate selected, from a group of materials consisting of: an oxide of the formula AO_x , where A is a material selected from the group consisting of Mo, W, Tc, Rh, Ir, Pd, In, Zn, Sn, Sr-Ru, Nd, Nb, Sm, La, V, and NaCl.

Response to Arguments

Applicant's arguments with respect to claims 21-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571)

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272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
29 May 2007

Zandra V. Smith
Zandra V. Smith
Supervisory Patent Examiner
29 May 2007